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L2	1611	716/5	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:09
L3	2048	716/4	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:09
L4	1	(716/6).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:11
L5	0	(716/5).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:11
L6	0	(716/4).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:11
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2. **Design for reducing alpha-particle-induced soft errors in ECL logic circuitry**
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3. **Historical trend in alpha-particle induced soft error rates of the Alpha™ microprocessor**
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30 April-3 May 2001 Page(s):259 - 265
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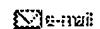
4. **A soft error immune 0.35 μm PD-SOI SRAM technology compatible with bulk CMOS**
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SOI Conference, 1998. Proceedings., 1998 IEEE International
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5. **High soft-error tolerance body-tied SOI technology with partial trench isolation (I generation devices)**
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VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on
11-13 June 2002 Page(s):48 - 49
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6. **Soft-error characteristics in bipolar memory cells with small critical charge**
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Electron Devices, IEEE Transactions on
Volume 38, Issue 11, Nov. 1991 Page(s):2465 - 2471
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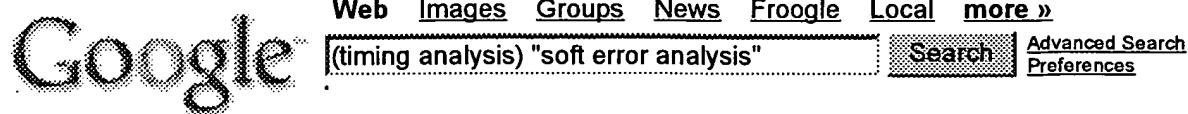
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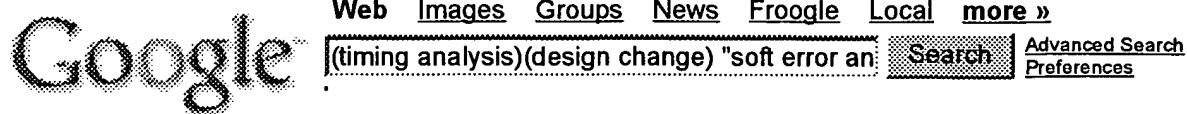
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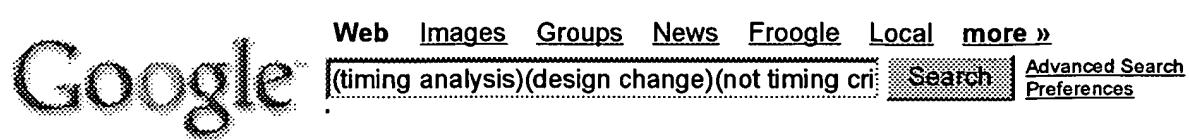
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